A New Empirical Nonlinear Model for Sub-250 nm Channel MOSFET

Alexandre Siligaris, Gilles Dambrine, *Member, IEEE*, Dominique Schreurs, *Senior Member, IEEE*, and François Danneville, *Member, IEEE*

***Abstract*—An empirical nonlinear model for sub-250 nm channel length MOSFET is presented which is useful for large signal RF circuit simulation. Our model is made of both analytical drain current and gate charge formulations. The drain current expression is continuous and infinitely derivable, and charge conservation is taken into account, as the capacitances derive from a single charge expression. The model's parameters are first extracted, prior the model's implementation into a circuit simulator. It is validated through dc, ac, and RF large signal measurements compared to the simulation.**

***Index Terms*—Charge conservation, large signal measurements, MOS transistors, nonlinear RF modeling.**

I. Introduction

MOSFET devices show very good RF performances, whenever applications with low power consumption are requested [1]. To this aim, designers need reliable RF small signal as well as nonlinear models, easy to extract and use. The existing ones are mainly physics based, or look-up table based. Physical models, like the well-known BSIM, are accurate, scalable both on the transistor's dimensions and technology, but generally the parameter's extraction is time consuming, requiring much technological data [2], [3]. On the other hand, look-up table models, showing accuracy and quick to extract, are not scalable and their use is limited to the measured operating range (in terms of voltage bias) [3].

The aim of this letter is to present an empirical nonlinear model for MOSFET easy to extract, scalable on gate width, which can be useful for applications like amplifiers, mixers, and oscillators down to the millimetric wave range. This model describes accurately the electrical (dc-ac) characteristics of MOS devices. It includes a nonlinear drain current expression that is continuous and infinitely derivable, leading to the transconductance and the output conductance to be continuous. The capacitances are derived directly from a gate charge expression that ensures the charge conservation principle [7]. In order to perform a validation of the model, large-signal simulations of bulk MOSFETs have been carried out and the measurements, using a Nonlinear Network Measurement System (NNMS), are compared to the simulations. Note that it is a general model for all MOS devices and it has been validated for SOI MOSFETs [4].

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A. Siligaris, G. Dambrine, and F. Danneville are with the IEMN CNRS UMR 8520, 59652 Villeneuve d'ASCQ, France (e-mail: alexandre.siligaris@iemn.univ-lille1.fr).

D. Schreurs is with the Div. ESAT-TELEMIC, K.U. Leuven, B-3001 Leuven, Belgium.

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II. Description and Extraction of the Model

The MOSFET model is presented in Fig. 1; it is similar to the one used in all FETs [3], [5]. The static drain current equation is originally based on the Angelov's model developed for III-V devices [6], but it has been modified in order to be suitable for MOS devices

$$\begin{aligned} I_{ds}(V_{gsi},V_{dsi}) =& I_{pk}W_f n_f\left[1+P(V_{gsi})\tanh\left(\Psi(V_{gsi})\right)\right]\times \\ &\times\left[P(V_{gdi})\tanh\left(V_{dsi}\left(K_7V_{gsi}+\alpha\right)\right)\right] \\ &\times\left[0.5\left(1+\tanh\left(10\left(V_{gsi}-V_{th}\right)\right)\right)\right] \\ \Psi\left(V_{gsi}\right) =& P_1\left(V_{gsi}-V_{pk}\right)+P_2\left(V_{gsi}-V_{pk}\right)^2 \\ &+P_3\left(V_{gsi}-V_{pk}\right)^3 \\ P(V_{gsi}) =& K_0+K_1V_{gsi}+K_2V_{gsi}^2+K_3V_{gsi}^3 \\ P(V_{gdi}) =& 1+K_4V_{gdi}+K_5V_{gdi}^2+K_6V_{gdi}^3. \end{aligned} \tag{1}$$

All terms P_i, K_i, α, V_{pk}, and I_{pk} are the model's parameters; W_f is the transistor's width per finger and n_f the number of fingers. V_{th} is the measured threshold voltage.

The transconductance and conductance equations are calculated by

$$\begin{aligned} g_{mi}(V_{gsi},V_{dsi}) =& \frac{\partial I_{ds}}{\partial V_{gsi}}_{|V_{dsi}=cte} \\ g_{di}(V_{gsi},V_{dsi}) =& \frac{\partial I_{ds}}{\partial V_{dsi}}_{|V_{gsi}=cte}. \end{aligned} \tag{2}$$

The model describes the static current versus the intrinsic voltages V_{gsi} and V_{dsi} (1), taking into account the potential drop across R_s and R_d.

The best way to model nonlinear capacitances and to ensure charge conservation, is to consider the total charge on a given physical point of a device [7], [8]. The charge on the gate electrode of a MOSFET depends on the gate bias and the drain bias, i.e., $Q_g = f(V_{gsi}, V_{dsi})$. The capacitance C_{gs} and C_{gd} are given by [7]

$$\begin{aligned} C_{gs}+C_{gd} =& \frac{\partial Q_g}{\partial V_{gsi}}_{|V_{dsi}=cte} \\ C_{gd} =& -\frac{\partial Q_g}{\partial V_{dsi}}_{|V_{gsi}=cte}. \end{aligned} \tag{3}$$

Using a gate charge to calculate C_{gs} and C_{gd}, we can model them without taking into account of a transcapacitance [7].

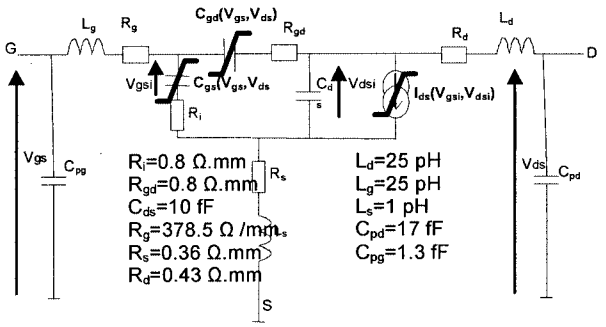

Fig. 1. Nonlinear model for the MOSFET. The values of the extrinsic and the linear intrinsic elements correspond to a bulk MOS with $L_g = 0.18\ \mu\mathrm{m}$ and $W_t = 6 * 8\ \mu\mathrm{m}$.

Following this principles, the gate charge for the MOS transistors was modeled by the following equation:

$$\begin{aligned} Q_g =& K\left(f_1(V_{gsi}, V_{dsi}) + f_2(V_{gsi}, V_{dsi})\right) \\ K =& C_0 n_f W_f \left(L_g - 2L_d\right) \\ f_1 =& \left(C_{gg1}V_{gsi} + C_{gg2}V_{gsi}^2 + C_{gg3}V_{gsi}^3\right) \\ & \times \left[C_{gg0} + \tanh\left(\frac{V_{dsi}^2}{\gamma V_{gsi}^2}\right)\right] \\ f_2 =& \left(C_{gd1}V_{gdi} + C_{gd2}V_{gdi}^2\right) \\ & \times \left[C_{gd0} + \tanh\left(-\frac{V_{dsi}}{V_\alpha}\right)\right]. \end{aligned} \tag{4}$$

In (4), L_g is the gate length, W_f the gate width per finger and n_f the number of fingers. C_0, L_d, C_{ggi}, C_{gdi}, γ and V_α are the model's parameters. The drain to source capacitance C_{ds} has a very low value and is being considered linear. The static gate current is neglected due to its very low value, thus the time-varying gate current $I_{gs}(t)$ is given by the following expression:

$$I_{gs}(t) = C_{pg}\frac{\partial V_{gs}(t)}{\partial t} + \frac{\partial Q_g(t)}{\partial t}. \tag{5}$$

To extract the overall parameters of the model, a set of dc measurements and a set of S-parameters measurements are required. First, we measure S-parameters over a large frequency range (0.5–50 GHz), for multibias points. The extrinsic elements (access resistances, inductances and pad capacitances) are extracted using the so "cold FET" method [9]. Then, the dc current parameters values are determined by adjusting the current's equation (1) on the measured dc current I_{ds}. Using the extrinsic elements values, a de-embedding procedure allows to extract the bias dependent intrinsic elements [3], [10]. This allows to determine the charge parameters which are extracted from the measured intrinsic capacitors C_{gs} and C_{gd}. This extraction procedure is implemented in ICCAP. Finally, the model is implemented in the ADS environment, in which all the simulations, shown in the next section, are performed.

III. Measurements-Results-Discussion

In order to validate the model, we present some results for a bulk MOS transistor owing a gate length $L_g = 0.18\ \mu\mathrm{m}$ and a gate width $W = 8 * 6\ \mu\mathrm{m}$. The static drain current as a function of the drain bias V_{ds}, is shown in Fig. 2. We observe

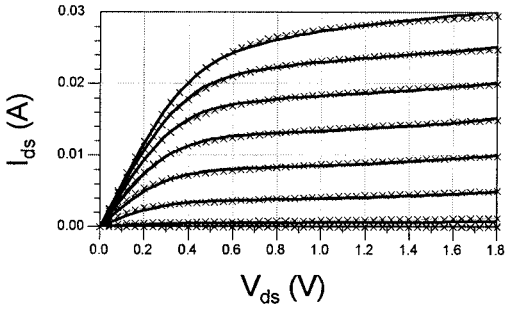

Fig. 2. Static drain current versus V_{ds} for different values of V_{gs} (0–1.8 V/0.2 V). Symbols correspond to the measurements and the solid line to the simulation.

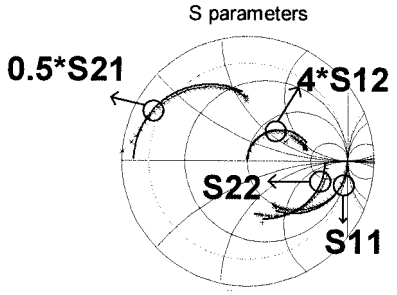

Fig. 3. Scattering parameters for frequencies from 500 MHz to 50 GHz. DC bias conditions are: $V_{ds0} = 1.8\ \mathrm{V}$, $V_{gs0} = 0.9\ \mathrm{V}$. Symbols are used for measurements and solid line for the simulation.

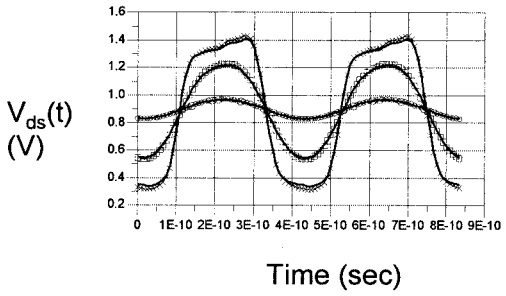

Fig. 4. Output voltage wave on the drain for three different input power values (-15 dBm, 0 dBm, 10 dBm). DC bias conditions: $V_{ds0} = 0.9\ \mathrm{V}$, $V_{gs0} = 0.9\ \mathrm{V}$. Symbols are used for measurements and solid line for the simulation.

a very good agreement on the dc characteristics. In Fig. 3, the measured and simulated S-parameters are shown for frequencies varying from 0.5 to 50 GHz. The model shows good description in small signal RF conditions. However, it is much more interesting to check the validity of the model through large signal measurements. For this purpose, we used an NNMS set-up and a sine-wave signal of 2.4 GHz has been applied to the gate of the MOSFET; which corresponds to a single tone measurement [11]. The loads at both gate and drain terminals are maintained to 50 Ω. The input power of the sine-wave signal varies between -15 dBm and 10 dBm. In Fig. 4 we illustrate the output voltage waveform $V_{ds}(t)$ corresponding to three values of the input sine-wave power (-15 dBm, 0 dBm, 10 dBm). Next, in Fig. 5 are shown the drain and the gate current wave forms for an input power of 10 dBm. It is shown that the large signal variations presented by the voltage and current signals are very well reproduced by the model, with a high accuracy. This is more evident in Fig. 6, where the output power is shown to be very

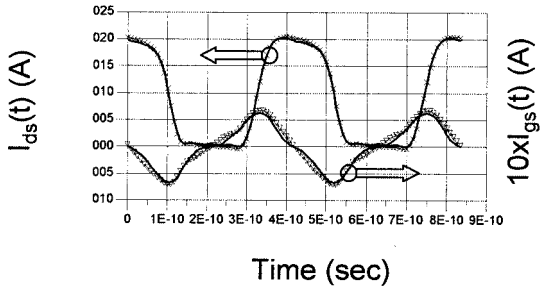

Fig. 5. Drain and gate (scaled 10 times) current wave forms. The input power signal is 10 dBm. DC bias conditions: $V_{ds0} = 0.9\,\mathrm{V}$, $V_{gs0} = 0.9\,\mathrm{V}$.

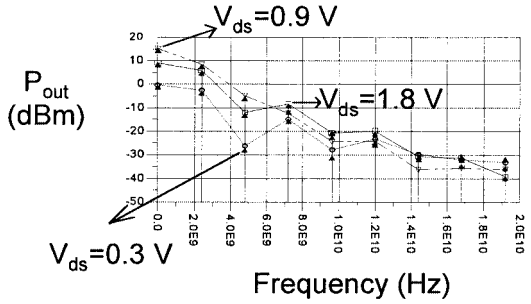

Fig. 6. Output power spectrum, up to the 8th harmonic, for an input power of 10 dBm and three drain bias values. The arrows show the simulation and the symbols with dotted lines show the measured spectrum. $V_{gs0} = 0.9\,\mathrm{V}$.

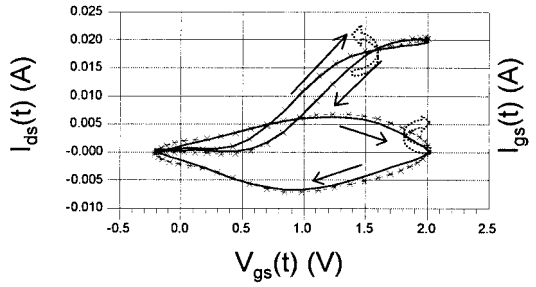

Fig. 7. Instantaneous drain current $\mathrm{I}_{ds}(\mathrm{t})$ and gate current $\mathrm{I}_{gs}(\mathrm{t})$ versus instantaneous gate voltage $\mathrm{V}_{gs}(\mathrm{t})$ for an input power of 10 dBm. This hysteresis is caused by the RC delays. The arrows show the time dependence path. $\mathrm{V}_{ds0} = 0.9\,\mathrm{V}$, $\mathrm{V}_{gs0} = 0.9\,\mathrm{V}$.

close to the experimental ones up to the 8th harmonic for three different drain bias values and an input power of 10 dBm. In addition, the input capacitance's nonlinearities are well described by the model, for the simulated dynamic gate current (Fig. 5) shows a good agreement with the measured one. Finally, this can be seen also through the hysteresis curve, on Fig. 7, which is caused by R-C delays; the instantaneous $I_{ds}(t)$ and $I_{gs}(t)$ currents versus the instantaneous $V_{gs}(t)$ signal are similar for the theoretical either the experimental results.

IV. Conclusion

An empirical nonlinear model, which is charge conservative, for MOS transistors, useful for large signal RF circuit simulation, has been presented. This model is a compromise between compact models and look-up table models, and combines some advantages of each modeling technique. The electric equivalent circuit is similar to those used for all FETs, it includes a nonlinear drain current expression and a nonlinear gate charge equation. The model shows very good dc and RF prediction of the nonlinearity's and the harmonics level.

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